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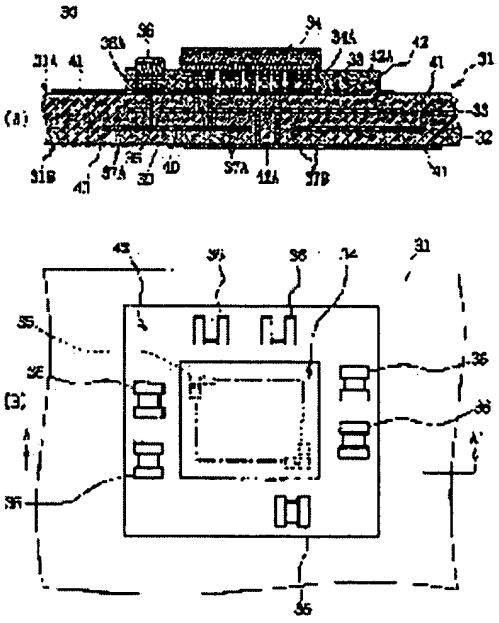
(54) MOUNTING BOARD, ELECTRONIC COMPONENT MOUNTING, AND SEMICONDUCTOR DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To enable practically sufficient reduction in layout spacing between electronic components at a point where noise prevention and high-density mounting are to be performed.

SOLUTION: Electrodes 35, 36A of electronic components 34, 36 are joined with lands 37A of a wiring board 31 via an anisotropic conductive member 42, and the electronic components 34, 36 and the wiring board 31 are held in an integral manner. Thus, since the spacing between the electronic components 34, 36 does not depend upon the cutting accuracy of the anisotropic conductive member 42 or the positioning accuracy with respect to the wiring board 31, the layout spacing between the electronic components 34, 36 may be significantly reduced. Thus, a mounting board, an electronic component mounting method and a semiconductor device which enable high-density mounting may be realized.



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CLAIMS

[Claim(s)]
[Claim 1] The mounting substrate characterized by having the anisotropy conductive member which holds each above-mentioned electronic parts and the above-mentioned wiring substrate at one while joining the wiring substrate in which the land corresponding to each electrode of two or more electronic parts and the electronic parts of the above-mentioned plurality [field / one] was prepared, and each above-mentioned electrode of each above-mentioned electronic parts to the above-mentioned land to which a wiring substrate is equivalent, respectively.
[Claim 2] The mounting substrate according to claim 1 characterized by having the insulating resin which covers the field [in which each above-mentioned electrode of each above-mentioned electronic parts is prepared], and field side which counters.
[Claim 3] The electronic-parts mounting method characterized by providing the following. The 1st process which produces the wiring substrate by which each electrode of two or more electronic parts was made to correspond, and the land was prepared in one field. The 2nd process which holds the electronic parts and the above-mentioned wiring substrate of the above-mentioned plurality to one through the above-mentioned anisotropy conductive member while joining each above-mentioned electrode of two or more above-mentioned electronic parts to the above-mentioned land to which the above-mentioned wiring substrate is equivalent through anisotropy conductive member, respectively.
[Claim 4] The electronic-parts mounting method according to claim 3 characterized by having the 3rd process which therefore covers two or more above-mentioned electronic parts to the insulating resin concerned by dropping an insulating resin from the field [in which each above-mentioned electrode of each above-mentioned electronic parts is prepared], and field side which counters.
[Claim 5] The semiconductor device characterized by to have the wiring substrate in which the land corresponding to each electrode of two or more electronic parts and the electronic parts of the above-mentioned plurality [field / one] was prepared, and the anisotropy conductive member which holds each above-mentioned electronic parts and the above-mentioned wiring substrate at one while joining each above-mentioned electrode of each above-mentioned electronic parts to the above-mentioned land to which a wiring substrate is equivalent, respectively in the semiconductor device mounted in one field of a wiring substrate.
[Claim 6] The semiconductor device according to claim 5 characterized by having the insulating resin which covers the field [in which each above-mentioned electrode of each above-mentioned electronic parts is prepared], and field side which counters.
[Claim 7] The above-mentioned wiring substrate is a semiconductor device according to claim 5 characterized by having the land prepared in the field of another side, and the electrical connecting means prepared on the above-mentioned land.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Table of Contents] this invention is explained in order of the following.
The technical field Prior art to which invention belongs (drawing 7 and drawing 8)
The 1st example of a gestalt (1) of implementation of technical-problem The-means-for-solving-a-technical-problem invention which invention tends to solve (drawing 1 and drawing 2)
(2) The 2nd example (drawing 3)
(3) Other examples (drawing 4 - drawing 6)
Effect-of-the-invention [0002]
[The technical field to which invention belongs] this invention is applied to one the mounting substrate and the electronic-parts mounting method of coming to mount a bare chip and a chip in a field, and semiconductor device of a multilayer-interconnection substrate, concerning a mounting substrate, the electronic-parts mounting method, and a semiconductor device, and is suitable.
[0003]
[Description of the Prior Art] Conventionally, in information processors, such as an engineering workstation (Engineering Work Station, EWS) and a personal computer, ****** and this kind of information processor has been miniaturized by improvement in semiconductor integration technology and mounting technology at the same time the throughput is therefore improving to promotion of parallel-processing-izing, and improvement in the speed of a clock rate.
[0004] Moreover, in this kind of information processor, the amount of information to deal with increased and the ****** system clock is also accelerated to this. Furthermore, ****** is used for improvement in information communication (network) technology, such as a cellular phone, ISDN (Integrated Services Digital Network, comprehensive digital communication service network), and a personal computer, and a RF communication block, velocity-of-light serial interface, etc. are used for various devices.
[0005] Thus, especially, in the information processing field or the information communication field, the ****** system is changing to informational digitization and improvement in the speed of a signal, and the reduction in a noise in the RF circuit block used for devices, such as the above personal computers, and a miniaturization of a device are desired. In order to realize such a request, bare chip mounting of a multi chip module (Multichip Module, MCM), flip chip mounting, etc. is used as the mounting method of a semiconductor chip.
[0006] Usually, it sets to flip chip mounting using the bare chip. After forming the bump who becomes with solder etc., respectively on two or more electrodes (this is hereafter called pad) formed in the circuit side of the bare chip concerned, By making the circuit side of a bare chip, and one field of a mother board counter, and joining each bump of a bare chip to the corresponding land arranged in one field of a mother board, respectively, it is made as [mount / a bare chip / in one field of the mother board concerned].
[0007] In addition, as a mother board in which a bare chip is mounted, the multilayer-interconnection substrate which comes to carry out laminating formation of the predetermined circuit pattern layer which becomes with copper etc., and the polyimide layer one by one is usually used for one field of the multilayer-interconnection substrate which comes to carry out laminating formation of ceramic substrates, such as the multilayer-interconnection substrate and alumina with which it comes to carry out the laminating of organic substrates, such as glass epoxy or a glass polyimide, and the predetermined circuit pattern one by one, or a mullite, and the predetermined circuit pattern one by one, or
[0008] By forming the bump who becomes with high-melting point solder on the pad of a bare chip as mounting by this flip chip, and performing a solder precoat on a mother board The solder flip chip method which connects each pad

of a bare chip, and each land to which a mother board is equivalent, After using the Au(gold) wirebonding method, forming Au bump on each pad of a bare chip and only a proper quantity's imprinting conductive pastes, such as Ag (silver) paste, on a bump, there is the conductive resin flip chip method which mounts a bare chip directly on a mother board.

[0009] An example of a mounting substrate by which the bare chip was therefore mounted in solder flip chip mounting here in one field of a mother board is shown in drawing 7 . As shown in drawing 7 (A) and drawing 7 (B), it sets to this mounting substrate 1. The pad 3 prepared in the outermost periphery of circuit side 2A of a bare chip 2 at the ****** predetermined pitch, [two or more] When the land 5 prepared in one field 4A of a mother board 4 corresponding to each [these] pad 3 joins through the bump 6 who becomes with high-melting point solder, the bare chip 2 is mounted in one field 4A of the mother board 4 concerned. Moreover, therefore in this mounting substrate 1, the chip 7 which are noise cure parts, such as resistance and a capacitor, is mounted in the land 5 corresponding to solder 8 in one field 4A of a mother board 4.

[0010] In this case, it comes by turns to carry out laminating formation of the predetermined circuit pattern layer 10 which a mother board 4 becomes with the ceramic substrate 9, copper, etc., and the solder resist 11 is formed in the predetermined field of one field 4A of the mother board 4 concerned, and field 4B of another side. Moreover, on each land 5 of one field 4A of a mother board 4, the solder precoat layer 12 which becomes by the eutectic solder is formed. Thereby, in this mounting substrate 1, at the time of a reflow, a reflow of the solder precoat layer 12 is carried out at the temperature which is a grade which does not fuse high-melting point solder and an eutectic solder fuses, and the fused solder precoat layer 12 is welded at each bump 6.

[0011] Moreover, in this mounting substrate 1, after a bare chip 2 is mounted in one field 4A of a mother board, the gap between one field 4A of the mother board 4 concerned and circuit side 2A of a bare chip 2 is filled up with the insulating resin 13, and a bare chip 2 is closed. It is made as [prevent / each bump's 6 breakage produced when it originates in the difference in the coefficient of thermal expansion of a mother board 4 and a bare chip 2 and stress concentrates on each bump 6 by this].

[0012] As shown in drawing 7 (B), when the insulating resin 13 is enclosed with the circumference of a bare chip 2 here, the element-placement keepout area 14 for preventing that a chip 7 therefore fixes to the insulating resin 13 is formed. In this case, since it becomes the enclosure mouth which encloses the insulating resin 13 concerned, element-placement keepout area 14A of the side which encloses the insulating resin 13 is formed greatly.

[0013] However, while the arrangement interval of the part bare chip 2 and chip 7 becomes large and packaging density falls as a result since it is necessary to form the element-placement keepout area 14 as mentioned above when it is flip chip mounting which therefore needs to close a bare chip 2 to the insulating resin 13 in this way, there is a possibility of spoiling reduction-ization of a noise. Since the decoupling capacitor and terminator which are noise cure parts are mounted in many cases at a bare chip 2 especially in the case of a digital circuit, while packaging density falls flip chip mounting to be closed according to the insulating resin 13 to a ****** case, there is a possibility of spoiling reduction-ization of a noise.

[0014] Then, the flip chip mounting method using the anisotropy electric conduction film (Annisotropic Conductive Film, ACF) as one method for solving such a problem is proposed. It is shown in drawing 8 which attaches the same sign and shows an example of the mounting substrate using the anisotropy electric conduction film (adhesives) to a corresponding point with drawing 7 here.

[0015] In this mounting substrate 20 on each pad 3 for example, circuit side 2A of the bare chip 2 with which the Au bump 21 was formed using the Au wirebonding method As opposed to the anisotropy electric conduction film 22 pasted up so that each land 5 prepared in one field 4A of a mother board 4 corresponding to the pad 3 might be covered For example, per [5-100] the sticking-by-pressure temperature of 100-240 [**], the sticking-by-pressure time of 50-40 [a second], and one bump By carrying out thermocompression bonding by the pressure of [g], the bare chip 2 is mounted in one field 4A of a mother board 4.

[0016] In this case, in the bare chip 2, on each pad 3 prepared in circuit side 2A, the BLM (Ball Limiting Metal) membrane layer 23 which comes to carry out laminating formation of the metal coat layer which becomes with titanium, platinum, and gold one by one is formed, and the Au bump 21 is formed on each BLM membrane layer 23 concerned, respectively. This BLM membrane layer 23 is made as [prevent / the diffusion to the Au bump's 21 pad 3]. It is made here as [join / electrically / the land 5 to which a mother board 4 is equivalent / to each pad 3 of a bare chip 2] by being joined to each land 5 of a mother board 4 through conductive particle 22A by which each bump 21 was uniformly distributed in the anisotropy electric conduction film 22 in this mounting substrate 20.

[0017]

[Problem(s) to be Solved by the Invention] By the way, by the flip chip mounting method using this anisotropy electric

conduction film, if the noise cure chip 7 is arranged as much as possible near the bare chip 2 in case alignment of the anisotropy electric conduction film 22 is carried out to one field 4A of a mother board 4 and tacking is performed, it will be thought that reduction-ization of high density assembly and a noise is realizable.
[0018] However, while cutting out the anisotropy electric conduction film 22 from a big anisotropy electric conduction film so that the position of the periphery section of an anisotropy electric conduction film may be arranged between a bare chip 2 and a chip 7 when it therefore mounts a bare chip 2 and a chip 7 in this method at a mother board 4, you have to position the end ****** anisotropy electric conduction film 22 to a mother board 4. In this case, the bare chip 2 and chip 7 which adjoin each other mutually The size error produced in case the anisotropy electric conduction film 22 of the size corresponding to each bare chip 2 is cut out from a big anisotropy electric conduction film, The locational error at the time of pasting up the cut-off anisotropy electric conduction film 22 concerned on one field 4A of a mother board 4 is taken into consideration. A problem with it difficult [to have to arrange at a bigger interval than these size error and a locational error, and to fully bring practically the arrangement interval of a bare chip 2 and a chip 7 close in the cure against a noise and the point which carries out high density assembly] is ******.
[0019] this invention was made in consideration of the above point, and tends to propose the mounting substrate, the electronic-parts mounting method, and semiconductor device which can carry out high density assembly.
[0020]
[Means for Solving the Problem] In order to solve this technical problem, while joining each electrode of each electronic parts to the land to which a wiring substrate is equivalent, respectively through anisotropy conductive member in this invention, each electronic parts and a wiring substrate are held to one. Since each electronic parts are arranged on anisotropy conductive member, it cannot be dependent on the cutting precision of anisotropy conductive member, and the positioning accuracy to a wiring substrate, and the interval of each electronic parts can narrow the arrangement interval of each electronic parts sharply.
[0021]
[Embodiments of the Invention] About a drawing, one example of this invention is explained in full detail below.
[0022] (1) In 1st example drawing 1 , 30 shows a mounting substrate as a whole, and it comes to carry out laminating formation of the circuit pattern layer 33 the glass epoxy-group board 32 and predetermined in a mother board 31 by turns. Land 37A corresponding to electrode 36A prepared in one field of the chip 36 as each pad 35 prepared in circuit side 34A of the bare chip 34 as electronic parts and electronic parts arranged around the bare chip 34 concerned is formed in one field 31A of this mother board 31 by **********ing for example, Cu (copper) foil, respectively. Moreover, two or more land 37B is formed by **********ing for example, Cu foil also to field 31B of another side of a mother board 31.
[0023] Moreover, on each land 37A, (Nickel nickel) / golden (Au) plating layer 38 is formed, and while reducing connection resistance with the Au bump 40 and land 37A which were formed through the BLM membrane layer 39 on each putt 35 of a bare chip 34 by this, it is made as [raise / the conductivity of the Au bump 40 and land 37A]. Moreover, the solder resist 41 is formed in the predetermined field of one field 34A of a mother board 34, and field 34B of another side.
[0024] In circuit side 34A of a bare chip 34, they are ******, for example, aluminum, and AlSi to the outermost periphery of the circuit side 34A concerned. Or AlSi Cu Two or more becoming pads 35 are formed (drawing 1 (B)), and the BLM membrane layer 39 is formed on each pad 35 concerned, respectively. Moreover, on the BLM membrane layer 39, the Au bump 40 is formed, respectively, and this BLM membrane layer 39 is made as [prevent / the diffusion to the Au bump's 40 pad 35].
[0025] One field 31A of a mother board 31 is pasted here so that the anisotropy electric conduction film 42 of the shape of an adhesive film which becomes by predetermined thickness may cover each land 37A, and this anisotropy electric conduction film 42 is made as [hold / a mother board 31, a bare chip 34, and a chip 36 / to one]. Into this anisotropy electric conduction film 42, conductive particle 42A of the grabby diameters about 2-10 [mum] carried out, such as Au and nickel, is uniformly distributed by the plastics ball, and each bump 35 of a bare chip 34 and electrode 36A of a chip 36 are electrically joined to land 37A to which a mother board 31 corresponds through this conductive particle 42A.
[0026] Moreover, as shown in drawing 1 (B), the size of the anisotropy electric conduction film 42 is selected by the size which can mount the chip 36 arranged around a bare chip 34 and the bare chip 34 concerned in one field 31A of a mother board 31 through the anisotropy electric conduction film 42 concerned.
[0027] The process which mounts a bare chip 34 and a chip 36 in one field 31A of a mother board 31 here is shown in drawing 2 . On the BLM membrane layer 39 of each pad 35 first prepared in circuit side 34A of a bare chip 34, for example, a wirebonding tool is used and the Au bump 40 is formed. Then, after producing a mother board 31, where

field 31B of another side of the mother board 31 concerned is therefore supported to the predetermined means for supporting 43, tacking of the anisotropy electric conduction film 42 set to one field 31A of a mother board 31 in a predetermined size which covers each land 37A is carried out. In this case, tacking of the anisotropy electric conduction film 42 concerned is carried out to one field 31A of a mother board 31 at the temperature below the glass-transition-point temperature of the anisotropy electric conduction film 42 (drawing 2 (A)).

[0028] Then, while adsorbing field 34B of another side which counters circuit side 34A of a bare chip 34 with the predetermined adsorber 44 and making circuit side 34A of a bare chip 34 counter one field 31A of a mother board 31 After positioning each pad 35 of a bare chip 34 to each land 37A to which a mother board 31 corresponds, Per [5-100] the sticking-by-pressure temperature of 100-240 [**], the sticking-by-pressure time of 5-40 [a second], and one bump Thermocompression bonding of the bare chip 34 is carried out to the anisotropy electric conduction film 42 on the thermocompression bonding conditions of the pressure about [g] (drawing 2 (B)).

[0029] Next, after positioning electrode 36A of a chip 36 to land 37A to which a mother board 31 corresponds, the chip 36 concerned is made to fix to one field 31A of a mother board 31 by carrying out thermocompression bonding of the chip 36 to the anisotropy electric conduction film 42 using the tool (not shown) which has a heating head on above-mentioned thermocompression bonding conditions (drawing 2 (C)). Bengbu 39 established in each pad 35 of a bare chip 34 at this time and electrode 36A of a chip 36, and land 37A to which a mother board 31 corresponds are electrically joined through conductive particle 42A which exists in the anisotropy electric conduction film 42. A bare chip 34 and a chip 36 are mounted in one field 31A of a mother board 31 mechanically and electrically in this way.

[0030] In the above composition in this mounting substrate 30 Since the position of the periphery section of the anisotropy electric conduction film 42 can be arranged on the outside of a chip 36 by having arranged the bare chip 34 and the chip 36 on the anisotropy electric conduction film 42 The positioning accuracy at the time of pasting up the cutoff precision at the time of cutting out the anisotropy electric conduction film 42 from one big anisotropy electric conduction film and the end ****** anisotropy electric conduction film 42 concerned to a mother board 31 can be sharply eased as compared with the conventional mounting substrate 20. Therefore, since it does not depend for the interval of a bare chip 34 and a chip 36 on the cutting precision of the anisotropy electric conduction film 42, and the positioning accuracy to a mother board 31, as compared with the conventional mounting substrate 20, the interval of a bare chip 34 and a chip 36 can be narrowed sharply.

[0031] Moreover, in this mounting substrate 30, since a bare chip 34 and a chip 36 can be mounted in a mother board 31 by the same method by having arranged the bare chip 34 and the chip 36 on the anisotropy electric conduction film 42, while being able to simplify a mounting process as compared with the case where a chip is mounted, by the method that a bare chip is separate, like the conventional mounting substrates 1 and 20, mounting time can be shortened.

[0032] Moreover, since a bare chip 34 and a chip 36 are electrically connected with land 37A to which a mother board 31 corresponds through conductive particle 42A in the anisotropy electric conduction film 42, a bare chip 34 and a chip 36 are connectable with this mounting substrate 30 by land 37A and low resistance to which a mother board 31 corresponds. Moreover, in this mounting substrate 30, while turning the part and the mounting substrate 30 which are not using solder by having arranged the bare chip 34 and the chip 36 on the anisotropy electric conduction film 42 lightweight, in case the disposal of the mounting substrate 30 concerned is carried out, abandonment of solder can be prevented.

[0033] Furthermore, by this mounting substrate 30, since the nickel/Au plating layer 38 is formed on each land 37A prepared in one field 31A of a mother board 31, while being able to reduce connection resistance with a bare chip 34 and a chip 36, and a mother board 31, each pad 35 of each land 37A of a mother board 31 and a bare chip 34 and conductivity with electrode 36A of a chip 36 can be raised.

[0034] While joining each pad 35 of a bare chip 34, and electrode 36A of a chip 36 to the land to which a mother board 31 is equivalent through the anisotropy electric conduction film 42, respectively according to the above composition By having held the bare chip 34 and the chip 36, and the mother board 31 to one through the anisotropy electric conduction film Since the positioning accuracy at the time of pasting up the cutting precision at the time of cutting out the anisotropy electric conduction film 42 from one big anisotropy electric conduction film and the end ****** anisotropy electric conduction film 42 concerned to a mother board 31 can be sharply eased as compared with the conventional mounting substrate 20 An interval with the chip 36 arranged around a bare chip 34 and the bare chip 34 concerned as compared with the conventional mounting substrate 20 can be narrowed sharply. Moreover, since a bare chip 34 and a chip 36 can be mounted to a mother board 31 by the same method, a mounting process can be simplified. The mounting substrate 30 and the mounting method of a low noise which can therefore carry out high density assembly to a simple process in this way are realizable.

[0035] (2) In drawing 3 which attaches and shows the same sign to a corresponding point with 2nd example drawing

1 , 50 shows a semiconductor device as a whole, and consists of chip-size packages with which the bare chip 31 and the chip 36 were mounted in one field 53A of the multilayer-interconnection substrate 53 which comes to carry out laminating formation of the glass epoxy-group board 51 and the predetermined circuit pattern layer 52 by turns through the anisotropy electric conduction film 42.

[0036] While this semiconductor device 50 is electrically joined to corresponding land 54A by which the Au bump 39 and electrode 36A of a chip 36 which were prepared on each pad 35 of a bare chip 34 were prepared in one field 53A of the multilayer-interconnection substrate 53 through conductive particle 42A which exists in the anisotropy electric conduction film 42, the bare chip 34 and the chip 36, and the multilayer-interconnection substrate 53 are held through the anisotropy electric conduction film 42 at one. Moreover, as for the bare chip 34 and the chip 36, in the case of this semiconductor device 50, therefore, the field side where electrode 36A of the circuit side 34A side of the bare chip 34 concerned, the field 34B side which counters, and a chip 36 counters with the field in which it is formed is covered by the epoxy resin 55.

[0037] Moreover, this semiconductor device 50 consists of so-called BGA (Ball Grid Array) by which the solder ball 56 was formed in the pitch about 0.3-1.0 [mm] on each land 54B prepared in field 53B of another side of the multilayer-interconnection substrate 53, and is made as [mount / in a mother board / it]. In this case, you may change land 54B by the side of field 53B of another side of the multilayer-interconnection substrate 53 into an unreserved state, without forming the solder ball 56 in each land 54B prepared in field 53B of another side of the multilayer-interconnection substrate 53.

[0038] In the above composition in this semiconductor device 50 Since the position of the periphery section of the anisotropy electric conduction film 42 can be arranged on the outside of a chip 36 by having arranged the bare chip 34 and the chip 36 on the anisotropy electric conduction film 42 The positioning accuracy at the time of pasting up the cutoff precision at the time of cutting out the anisotropy electric conduction film 42 from one big anisotropy electric conduction film and the end ****** anisotropy electric conduction film 42 concerned to the multilayer-interconnection substrate 53 can be sharply eased as compared with the conventional semiconductor device. Therefore, since it does not depend for the interval of a bare chip 34 and a chip 36 on the cutting precision of the anisotropy electric conduction film 42, and the positioning accuracy to the multilayer-interconnection substrate 53, as compared with the conventional semiconductor device, the interval of a bare chip 34 and a chip 36 can be narrowed sharply.

[0039] Moreover, in this semiconductor device 50, since a bare chip 34 and a chip 36 can be mounted to the multilayer-interconnection substrate 53 by the same method by having arranged the bare chip 34 and the chip 36 on the anisotropy electric conduction film 42, while being able to simplify a mounting process as compared with the conventional mounting method, mounting time can be shortened sharply. Moreover, since a bare chip 34 and a chip 36 are electrically connected with land 54A to which the multilayer-interconnection substrate 53 corresponds through conductive particle 42A in the anisotropy electric conduction film 42, a bare chip 34 and a chip 36 are connectable with this semiconductor device 50 by land 54A and low resistance to which the multilayer-interconnection substrate 53 corresponds.

[0040] Moreover, in this semiconductor device 50, while turning the part and semiconductor device 50 which are not using solder by having arranged the bare chip 34 and the chip 36 on the anisotropy electric conduction film 42 lightweight, in case the disposal of the semiconductor device 50 concerned is carried out, abandonment of solder can be prevented. Moreover, in this semiconductor device 50, since the nickel/Au plating layer 38 is formed on each land 54A prepared in one field 53A of the multilayer-interconnection substrate 53, while being able to reduce connection resistance with a bare chip 34 and a chip 36, and the multilayer-interconnection substrate 53, each pad 35 of each land 54A of the multilayer-interconnection substrate 53 and a bare chip 34 and conductivity with electrode 36A of a chip 36 can be raised.

[0041] Moreover, in this semiconductor device 50, since packaging density of a semiconductor device 50 can be made high-density as compared with the conventional semiconductor device, the packaging density of a semiconductor device 50 to a mother board can be raised. Furthermore, with this semiconductor device 50, since the bare chip 34 and the chip 36 are therefore covered by the epoxy resin 55, a semiconductor device 50 can be protected from the exterior.

[0042] According to the above composition, by having arranged the bare chip 34 and the chip 36 on the anisotropy electric conduction film 42 Since the positioning accuracy at the time of pasting up the cutoff precision at the time of cutting out the anisotropy electric conduction film 42 from one big anisotropy electric conduction film and the end ****** anisotropy electric conduction film 42 concerned to the multilayer-interconnection substrate 53 can be sharply eased as compared with the conventional semiconductor device An interval with the chip 36 arranged around a bare chip 34 and the bare chip 34 concerned as compared with the conventional semiconductor device can be narrowed sharply. The semiconductor device 50 of a low noise which can therefore carry out high density assembly to a simple

process in this way is realizable.
[0043] (3) Although the mounting substrate 30 by which the bare chip 34 and the chip 36 have been arranged on the anisotropy electric conduction film 42 was described in other examples, in addition above-mentioned examples As this invention is shown not only in this but in drawing 4 , the field [in which electrode 36A of the circuit side 34A side of a bare chip 34, the field side which counters, and a chip 36 is formed], and field side which counters For example, even if it makes it cover therefore to an epoxy resin 61, the same effect as an above-mentioned example can be acquired.
[0044] The process which forms this epoxy resin 61 is performed by stiffening it, after the liquefied resin (for example, epoxy resin) of the hypoviscosity after performing the process shown in drawing 2 (C) is dropped using a dispenser etc. on the field in which electrode 36A of circuit side 34A of a bare chip 34, the field which counters, and a chip 36 is formed, and the field which counters. Thereby, since a bare chip 34 and a chip 36 are therefore closed by the epoxy resin 61, the mounting substrate 30 can be protected from the exterior.
[0045] Moreover, in an above-mentioned example, although the case where this invention was applied to the semiconductor device 50 which consists of chip-size packages was described, as shown in drawing 5 which attaches and shows the same sign to a corresponding point not only with this but drawing 3 , even if this invention applies this invention to the multi chip module type semiconductor device 70, it can acquire the same effect as an above-mentioned example.
[0046] As shown in drawing 5 , a semiconductor device 70 Each pad 35 of a bare chip 34, and electrode 36A of a chip 36, Corresponding land 74A prepared in one field 73A of the multilayer-interconnection substrate 73 which comes to carry out laminating formation of the glass epoxy-group board 71 and the predetermined circuit pattern layer 72 by turns By being electrically joined through conductive particle 42A in the anisotropy electric conduction film 42, the bare chip 34 and the chip 36 are mounted and constituted by one field 73A of the multilayer-interconnection substrate 73. In this case, therefore, you may close a bare chip 34 and a chip 36 to an epoxy resin 61 like the above-mentioned semiconductor device 50.
[0047] Moreover, in the case of this semiconductor device 70, it consists of so-called BGA by which the solder ball 75 which becomes by Cu was formed in the predetermined pitch on each land 74B of the multilayer-interconnection substrate 73 prepared in 73B on the other hand, and is made as [mount / in a mother board / it]. You may change each land 74B by the side of field 73B of another side of the multilayer-interconnection substrate 73 into an unreserved state, without forming the solder ball 75 here on each land 74 of the multilayer-interconnection substrate 73 prepared in 73B on the other hand.
[0048] As furthermore shown in drawing 6 , in a semiconductor device 70, it may replace with the solder ball 75 and field 73B of another side of the multilayer-interconnection substrate 73 may be equipped with the pin type connector 76. In this case, the pin type connector 76 is electrically connected with each land 74B prepared in field 73B of another side of the multilayer-interconnection substrate 73. Therefore, in case a semiconductor device 70 is mounted in a mother board, while being able to deal with the semiconductor device 70 concerned easily, the semiconductor device 70 concerned is easily exchangeable. This pin type connector 76 can be applied also to a semiconductor device 50, and can acquire the same effect.
[0049] Moreover, in an above-mentioned example, although the case where a chip 36 was mounted in a mother board 31 was described after mounting a bare chip 34 in a mother board 31, after mounting not only this but the chip 36 in a mother board 31, even if this invention is made to mount a bare chip 34 in a mother board 31, it can acquire the same effect as an above-mentioned example. Moreover, in an above-mentioned example, although the case where a bare chip 34 and a chip 36 were separately mounted in a mother board 31 was described, this invention may bundle up not only this but a bare chip 34 and a chip 36, and may mount them in a mother board 31. In this case, since a bare chip 34 and a chip 36 can be mounted in a mother board 31 at the same process, while being able to simplify a mounting process much more, mounting time can be shortened much more.
[0050] Moreover, although the case where carried out thermocompression bonding of a bare chip 34 and the chip 36 to the mother board 31, and they were mounted in it was described in the above-mentioned example after carrying out tacking of a bare chip 34 and the chip 36 to a mother board 31 at the temperature below the glass-transition-point temperature of the anisotropy electric conduction film 42 this invention carries out tacking not only of this but a bare chip 34 and a chip 36 to a mother board 31 at the temperature below the glass-transition-point temperature of the anisotropy electric conduction film 42. After ******, these bare chips 34 and a chip 36 are put in block, and it may be made to carry out thermocompression bonding of the continuity test and operation test of a bare chip 34 and a chip 36. Thereby, generating of the defective of the mounting substrate 30 can be prevented beforehand.
[0051] moreover, it sets in the above-mentioned example, although the case where thermocompression bonding of a bare chip 34 and the chip 36 was carried out to the anisotropy electric conduction film 42 on the sticking-by-pressure

temperature of 100-240 [**], the sticking-by-pressure time of 5-40 [a second], and the thermocompression bonding conditions of the pressure about per [5-10] one bump [g] was described As long as this invention can, in short, carry out thermocompression bonding of a bare chip 34 and the chip 36 to the anisotropy electric conduction film 42 not only in this, it may carry out thermocompression bonding of a bare chip 34 and the chip 36 to the anisotropy electric conduction film 42 on various thermocompression bonding conditions.

[0052] Moreover, in an above-mentioned example, as a wiring substrate by which the land corresponding to each electrode of two or more electronic parts was prepared in one field, although the case where a mother board 34, the multilayer-interconnection substrate 53, and the multilayer-interconnection substrate 73 were used was described this invention as a wiring substrate by which the land corresponding to each electrode of two or more electronic parts was prepared in one [not only this but] field Organic wiring substrates, such as a paper epoxy-group board, an aramid substrate, a polyimide substrate, and a bismaleido triazine (BT)-resin substrate, Various wiring substrates, such as wiring substrates, such as ceramic multilayer-interconnection substrates, such as an alumina, a mullite, and a glass ceramic, and Cu / polyimide wiring substrate on a silicon substrate, can be applied.

[0053] Moreover, although the case where the anisotropy electric conduction film 42 was used as anisotropy conductive member which holds each electronic parts and a wiring substrate to one was described while joining each electrode of each electronic parts to the land to which a wiring substrate is equivalent, respectively in the above-mentioned example While this invention joins each electrode of not only this but each electronic parts to the land to which a wiring substrate is equivalent, respectively As anisotropy conductive member which holds each electronic parts and a wiring substrate to one, for example, the paste-like anisotropy electric conduction film with which it comes to mix a thermosetting epoxy resin, a thermoplastic rubber system resin, a conductive particle, and a solvent, For example, you may use the anisotropy electric conduction film with which metal particles, such as Au and nickel, were distributed. When using paste-like anisotropy conductive member, it may form in one field 34A of a mother board 31 using screen printing, or may be directly dropped at a plane of composition using a dispenser etc.

[0054] Moreover, although the case where epoxy resins 55 and 61 were used as an insulating resin which covers the field [in which the electrode of each electronic parts is prepared], and field side which counters in an above-mentioned example was described, in addition to this, this invention can apply various insulating resins as an insulating resin which covers the field [in which the electrode of not only this but each electronic parts is prepared], and field side which counters. In a further above-mentioned example, although the case where the solder balls 56 and 75 and the pin type connector 76 were used as electrical connecting means prepared on the land was described, in addition to this, this invention can apply various electrical connecting means as electrical connecting means prepared not only this but on the land.

[0055]

[Effect of the Invention] Since it does not depend for the interval of each electronic parts on the cutting precision of anisotropy conductive member, and the positioning accuracy to a wiring substrate by having held each electronic parts and the wiring substrate to one while joining each electrode of each electronic parts to the land to which a wiring substrate is equivalent, respectively through anisotropy conductive member as mentioned above according to this invention, the arrangement interval of each electronic parts can be narrowed sharply. The mounting substrate, the electronic-parts mounting method, and semiconductor device which can carry out high density assembly in this way are realizable.

[Translation done.]

* NOTICES *

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damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

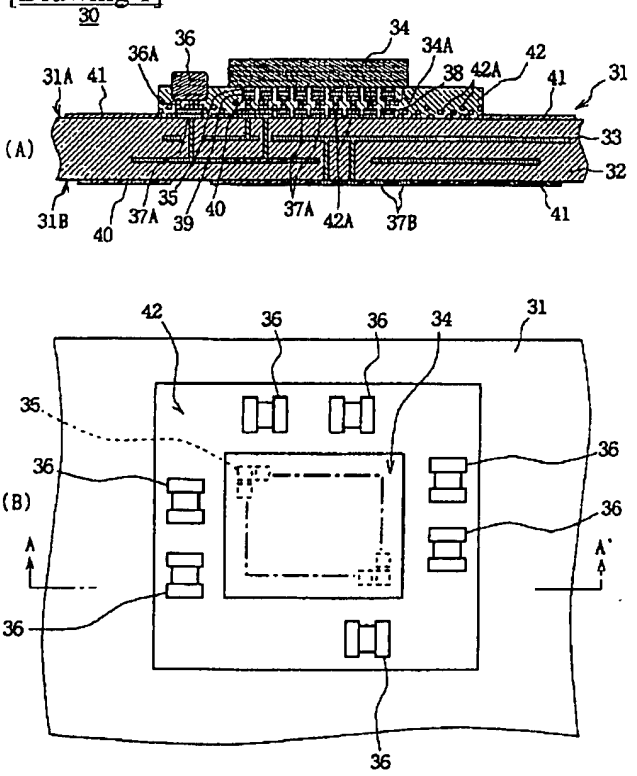


図１　実施例による実装基板の構成

[Drawing 2]

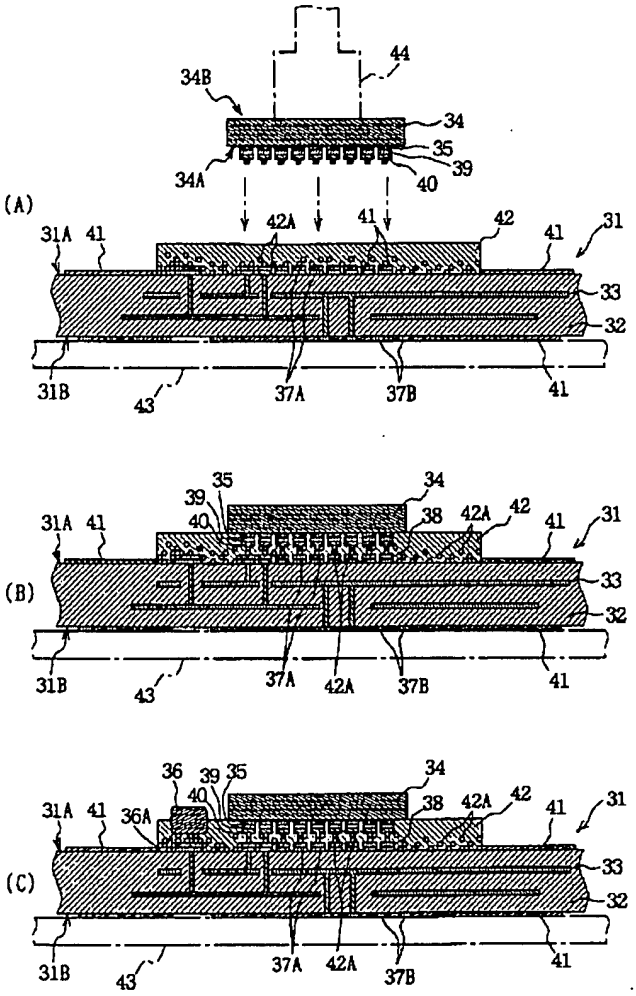


図２　実装基板の製造工程

[Drawing 3]

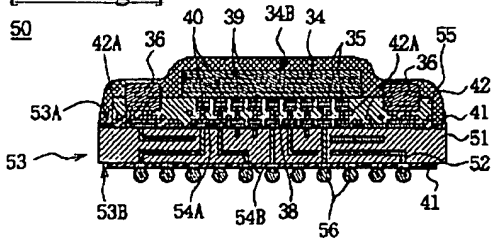


図３　実施例による半導体装置の構成

[Drawing 4]

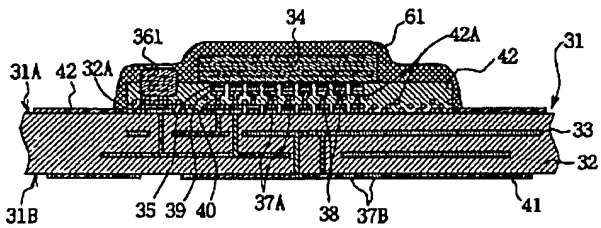


図４　他の実施例による実装基板の構成

[Drawing 5]

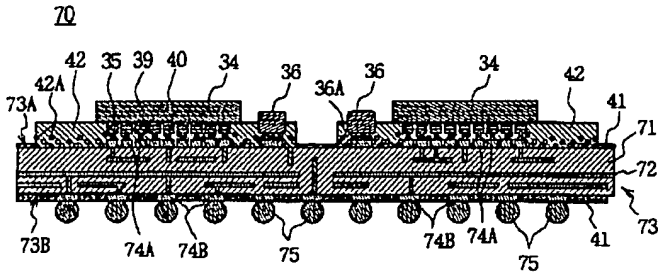


図５　他の実施例による半導体装置の構成

[Drawing 6]

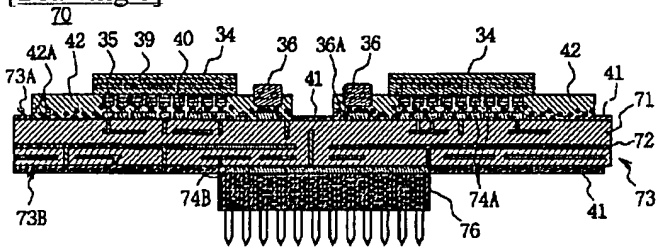
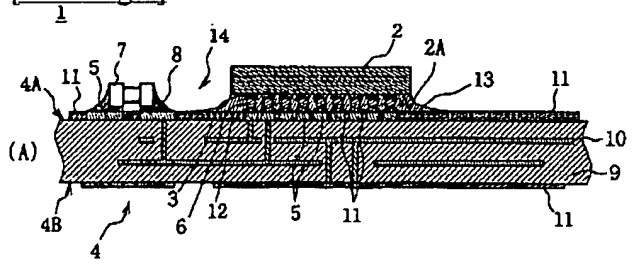


図６　他の実施例による半導体装置の構成

[Drawing 7]



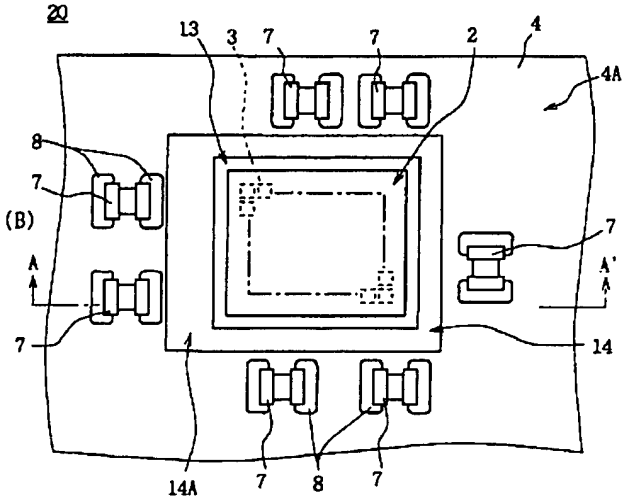


図７　従来の実装基板の一構成例

[Drawing 8]

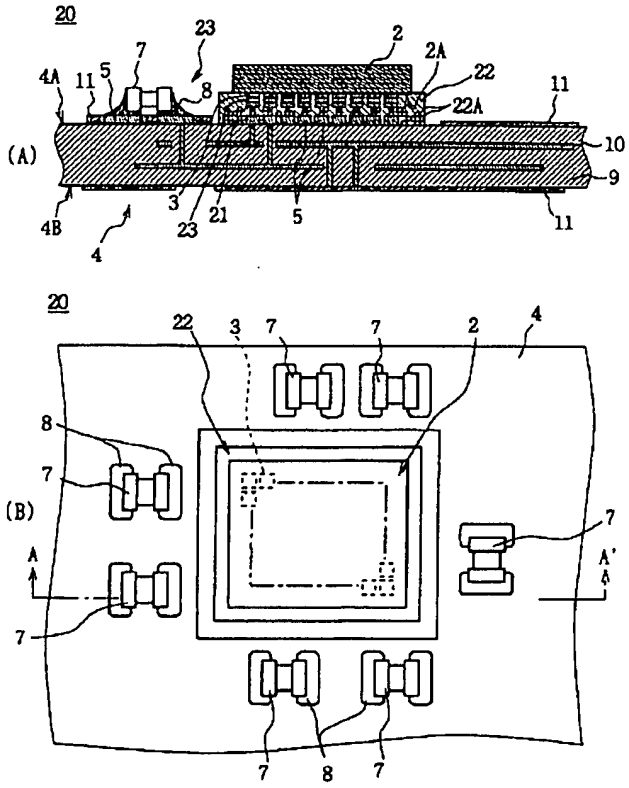


図８　異方性導電フィルムを用いた従来の実装基板の一構成例

[Translation done.]